DOCKET NO. MULLER 7-7 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

David Muller, et al.

Serial No.: N/A

Filed: Herewith

For: A SILICON OXIDE BASED GATE DIELECTRIC LAYER

Group No.: N/A

Examiner: N/A

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Sir:

INFORMATION DISCLOSURE STATEMENT

Pursuant to the duty of disclosure under 37 C.F.R. § 1.56, Applicant submits this statement. This submittal is made in accordance with 37 C.F.R. §§ 1.97 and 1.98 and § 609 of the Manual of Patent Examining Procedure. The patents, publications and other information herein are listed below and on the attached Form PTO-1449. Copies of the listed references are submitted herewith.

U.S. Patent No.	Inventor	Date
6,251,800 B1	Sun et al.	June 26, 2001
4,783,238	Roesner	November 8, 1988
2002/004715 A1	Kim et al.	April 25, 2002

References:

Kei-ichi Yamaguchi, Shigeru Imai, Naoto Ishitobi, Masashi Takemoto, Hidejiro Miki, and Masakiyo Matsumura; "ATOMIC-LAYER CHEMICAL-VAPOR-DEPOSITION OF SILICON DIOXIDE FILMS WITH AN EXTREMELY LOW HYDROGEN CONTENT"; June 1998, Applied Surface Science, Vol. 130-132, Pgs. 202-207.

J.W. Klaus, O. Sneh, A.W. Ott and S.M. George; "ATOMIC LAYER DEPOSITION OF SiO2 USING CATALYZED AND UNCATALYZED SELF-LIMITING SURFACE REACTIONS"; June-Aug. 1999; World Scientific, Surface Review and Letters, Vol. 6, Nos. 3 & 4, Pgs. 435-448.

D.A. Muller, T. Sorsch, S. Moccio, F.H. Baumann, K. Evans-Lutterodt & G. Timp; "THE ELECTRONIC STRUCTURE AT THE ATOMIC SCALE OF ULTRATHIN GATE OXIDES"; 24 June 1999; Macmillan Magazines Ltd., Nature, Vol, 399; Pgs. 758-761.

Leonello Dori, Alexandre Acovic, Donelli J. DiMaria and Ching, Hsiang Hsu; "OPTIMIZED SILICON-RICH OXIDE (SRO) DEPOSITION PROCESS FOR 5-V-ONLY FLASH EEPROM APPLICATIONS"; June 1993, IEEE Electron Device Letters, Vol, 14, No. 6; Pgs. 283-285.

J.B. Neaton, D.A. Muller and N.W. Ashcroft; "ELECTRONIC PROPERTIES OF THE Si/SiO2 INTERFACE FROM FIRST PRINCIPLES"; The American Physical Society, Volume 85, Number 6, 7 August 2002; Pgs. 1298-1301.

David A. Muller, et al.; Serial No. 09/773,443 filed on October 2, 2003; "SILICON OXIDE BASED GATE DIELECTRIC LAYER".

Applicant hereby expressly reserves the right to swear behind the effective dates of any of the above Patents and to question the relevance and materiality of the Patents and Publications listed herein, in whole, in part, or in combination, subsequent to filing this Information Disclosure Statement. The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 08-2395.

Respectfully submitted,
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PTO/SB/08A (08-03)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	N/A
Filing Date	Herewith
First Named Inventor	David Muller, et al.
Art Unit	N/A
Examiner Name	N/A
Attorney Docket Number	MULLER 7-7

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 6,251,800 B1	06 26 2001	Sun et al.	
		US- 4,783,238	11 08 1988	Roesner	
		US- 2002/0047151 A1	04 25 2002	Kim et al.	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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(Use as many sheets as necessary)

Sheet 2 of 2

Compl te if Kn wn	
Application Number	N/A
Filing Date	Herewith
First Named Inventor	David Muller, et al.
Art Unit	N/A
Examiner Name	N/A
Attorney Docket Number	MULLER 7-7

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Kei-Ichi Yamaguchi, Shigeru Imai, Naoto Ishitobi, Masashi Takemoto, Hidejiro Miki, and Masakiyo Matsumura; "ATOMIC-LAYER CHEMICAL-VAPOR-DEPOSITION OF SILICON DIOXIDE FILMS WITH AN EXTREMELY LOW HYDROGEN CONTENT"; June 1998, Applied Surface Science, Vol. 130-132, Pgs. 202-207.	
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		D.A. Muller, T. Sorsch, S. Moccio, F.H. Baumann, K. Evans-Lutterodt & G. Timp; "THE ELECTRONIC STRUCTURE AT THE ATOMIC SCALE OF ULTRATHIN GATE OXIDES"; 24 June 1999; Macmillan Magazines Ltd., Nature, Vol, 399; Pgs. 758-761.	
		Leonello Dori, Alexandre Acovic, Donelli J. DiMaria and Ching, Hsiang Hsu; "OPTIMIZED SILICON-RICH OXIDE (SRO) DEPOSITION PROCESS FOR 5-V-ONLY FLASH EEPROM APPLICATIONS"; June 1993, IEEE Electron Device Letters, Vol, 14, No. 6; Pgs. 283-285.	
		J.B. Neaton, D.A. Muller and N.W. Ashcroft; "ELECTRONIC PROPERTIES OF THE Si/SiO2 INTERFACE FROM FIRST PRINCIPLES"; The American Physical Society, Volume 85, Number 6, 7 August 2002; Pgs. 1298-1301.	
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